Roll: 2221139

Guru Nanak Dev Engineering College, Ludhiana

Department of Information Technology

Program	B.Tech.(IT)	**Semester**	3
Subject Code	ESIT-101	**Subject Title**	DCLD
Mid Semester Test (MST) No.	1	**Course Coordinator(s)**	Harpreet Kaur
Max. Marks	24	**Time Duration**	1 hour 30 minutes
Date of MST		**Roll Number**	

Note: Attempt all questions

Q. No.	Question	COs, RBT level	Marks
Q1	Justify the use of Gray codesin Digital electronics.	CO2. L2	2
Q2	Explain De Morgan's theorem.	CO2. L4	2
Q3	What are Universal gates? Realize following gates using Universal gates a) Ex-OR b) OR	CO3. L3	2+2
Q4	Describe SOP and POS forms? How to convert one form to another.	CO2. L4	4
Q5	Convert following: (a) $(218.6)_{10} = (\ )_{16}$ (DA·98)16 (b) $(110100.1101)_2 = (\ )_8$ (64·64)8	CO1. L4	2+2
Q6	(a) Minimize following Boolean function using K-Map. f = m(1,4, 5, 6, 11, 12, 13, 14) f = bc' + bd' + a'c'd + ab'cd (b) Minimize following Boolean function using Boolean laws F = AB + (AC)' + AB'C(AB + C) = ~~B+C~~ A'C B+A' => 1	CO2.CO3. L5	4+4

Course Outcomes (CO)

Students will be able to

1	To understand and examine the structure of various number systems and its application in digital design
2	Utilize knowledge of number systems, codes and Boolean algebra to the analysis and design of digital logic circuits
3	Formulate and employ a Karnaugh Map to reduce Boolean expressions and logic circuits to their simplest forms
4	Identify concepts and terminology of digital logic circuits
5	Ability to understand, analyze and design various combinational and sequential circuits
6	To develop skill to build, and troubleshoot digital circuit

RBT Classification	Lower Order Thinking Levels (LOTS)			Higher Order Thinking Levels (HOTS)		
RBT Level Number	L1	L2	L3	L4	L5	L6
RBT Level Name	Remembering	Understanding	Applying	Analyzing	Evaluating	Creating

Guru Nanak Dev Engineering College, Ludhiana			
Department of Information Technology			
Program	B.Tech.(IT)	**Semester**	3
Subject Code	ESIT-101	**Subject Title**	DCLD
Mid Semester Test (MST) No.	2	**Course Coordinator(s)**	Harpreet Kaur
Max. Marks	24	**Time Duration**	1 hour 30 minutes
Date of MST		**Roll Number**	

Note: Attempt all questions

Q. No.	Question	COs, RBT level	Marks
Q1	Differentiate Combinational and Sequential circuits.	CO5, L2	2
Q2	Describe Race around condition in JK Flip Flop and How to remove it.	CO5, L4	2
Q3	Explain the working of 4:2 Encoder. Also list the Application areas of Encoder.	CO5, L2	3+1
Q4	Illustrate the need and working of Carry Look ahead Adder.	CO5, L3	4
Q5	What is the difference between Latch and Flip Flop. Design and implement SR Flip Flop.	CO5, L4	2+2
Q6	Design 2 bit Synchronous Up counter using JK flip flop.	CO5, CO6, L5	8

Course Outcomes (CO)
Students will be able to

1	To understand and examine the structure of various number systems and its application in digital design
2	Utilize knowledge of number systems, codes and Boolean algebra to the analysis and design of digital logic circuits
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RBT Level Number	L1	L2	L3	L4	L5	L6
RBT Level Name	Remembering	Understanding	Applying	Analyzing	Evaluating	Creating

Guru Nanak Dev Engineering College, Ludhiana			
Department of Information Technology			
Program	B.Tech.(IT)	**Semester**	3
Subject Code	ESIT-101	**Subject Title**	DCLD
Mid Semester Test (MST) No.	1	**Course Coordinator(s)**	Harpreet Kaur
Max. Marks	24	**Time Duration**	1 hour 30 minutes
Date of MST		**Roll Number**	

Note: Attempt all questions

Q. No.	Question	COs, RBT level	Marks
Q1	What are gray codes?	CO1, L2	2
Q2	Explain De Morgan's theorem.	CO2, L5	2
Q3	What are universal gates? Realize following gates using universal gates a) Ex-OR b) AND	CO3, L3	4
Q4	What are SOP and POS forms? How to convert one form to another.	CO2, L3	4
Q5	Convert following: a) $(28.7)_{10} = (\ )_{16}$ b) $(111100.111)_2 = (\ )_8$	CO4, L5	4
Q6	Minimize following Boolean function using K-Map. $f = m(1, 5, 6, 11, 12, 13, 14)$	CO3, L6	8

Course Outcomes (CO)

Students will be able to

1	Design sequential circuits using Boolean algebra.
2	Explain the Memory Organization and its classification.
3	Use the techniques, skills, and modern engineering tools such as logic works necessary for engineering practice.
4	Use the techniques, skills, and modern engineering tools such as logic works necessary for engineering practice.
5	Design combinational and sequential circuits using Boolean algebra.
6	Design sequential circuits using Boolean algebra.

RBT Classification	Lower Order Thinking Levels (LOTS)			Higher Order Thinking Levels (HOTS)		
RBT Level Number	L1	L2	L3	L4	L5	L6
RBT Level Name	Remembering	Understanding	Applying	Analyzing	Evaluating	Creating

Guru Nanak Dev Engineering College, Ludhiana			
Department of Information Technology			
Program	B.Tech.(IT)	**Semester**	3
Subject Code	ESIT-101	**Subject Title**	DCLD
Mid Semester Test (MST) No.	2	**Course Coordinator(s)**	Harpreet Kaur
Max. Marks	24	**Time Duration**	1 hour 30 minutes
Date of MST		**Roll Number**	

Note: Attempt all questions

Q. No.	Question	COs, RBT level	Marks
Q1	Describe synchronous and asynchronous counters.	CO1, L2	2
Q2	Compare Level and edge triggering of clock.	CO4, L4	2
Q3	Describe shift registers. Explain PISO and SIPO shift registers.	CO4, L2	4
Q4	Illustrate the need and working of Carry look ahead adder.	CO4, L3	4
Q5	Design and implement a 4-bit binary to gray convertor.	CO6, L6	4
Q6	Design 2 bit Synchronous Up counter using JK flip flop.	CO3, L6	8

Course Outcomes (CO)

Students will be able to

1	Design sequential circuits using Boolean algebra.
2	Explain the Memory Organization and its classification.
3	Use the techniques, skills, and modern engineering tools such as logic works necessary for engineering practice.
4	Use the techniques, skills, and modern engineering tools such as logic works necessary for engineering practice.
5	Design combinational and sequential circuits using Boolean algebra.
6	Design sequential circuits using Boolean algebra.

RBT Classification	**Lower Order Thinking Levels (LOTS)**			**Higher Order Thinking Levels (HOTS)**		
RBT Level Number	L1	L2	L3	L4	L5	L6
RBT Level Name	Remembering	Understanding	Applying	Analyzing	Evaluating	Creating

Please check that this question paper contains____09__ questions and _2____ printed pages within first ten

[Total No. of Questions: 09] [Total No. of Pages: .....]

Uni. Roll No. .....

MORNING

27 DEC 2022

Program: B.Tech. (Batch 2018 onward)

Semester: 3rd

Name of Subject: Digital Circuits and Logic Design

Subject Code: ESIT-101

Paper ID: 16042

Time Allowed: 03 Hours **Max. Marks: 60**

NOTE:

1) Parts A and B are compulsory
2) Part-C has Two Questions Q8 and Q9. Both are compulsory, but with internal choice
3) Any missing data may be assumed appropriately

Part – A **[Marks: 02 each]**

Q1.

a) Define 1's complement and 2's complement.

b) What are the various uses of VHDL?

c) Illustrate the advantages of Ring Counter.

d) Write a short note on SOP and POS.

e) Convert $(10101)_2$ to decimal. →

f) Compare encoder and decoder.

Part – B **[Marks: 04 each]**

Q2. State and prove De-Morgan's Theorem.

Q3. What are universal gates? Realize the following gates using universal gates:

a. AND b. EX-NOR

Q4. Illustrate the working of Master Slave J-K flip flop.

Q5. Reduce the following Boolean expression: x'y'z +yz+ xz.

Q6. What is full subtractor? Draw a full subtractor circuit.

P.T.O.

MORNING

27 DEC 2022

Q7. Explain the working of Gray code. Write its importance and its uses.

Part – C

[Marks: 12 each]

Q8. Write short note on following:

a. RTL logic family **(6 marks)**

b. R-2R Ladder **(6 marks)**

OR

Design an 8 ×1 multiplexer using 4×1 and 2×1 multiplexer.

Q9. Design 2-bit Synchronous Up counter using JK flip flop.

OR

Minimize the following Boolean function-

$F(A, B, C, D) = \Sigma m(1, 3, 4, 6, 8, 9, 11, 13, 15) + \Sigma d(0, 2, 14)$

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Please check that this question paper contains 09 questions and 01 printed pages within first ten minutes.

[Total No. of Questions: 09] [Total No. of Pages: 01]

Uni. Roll No. .....

Program: B.Tech. (IT)

Semester: 3rd

Name of Subject: Digital Circuits and Logic Design

Subject Code: ESIT-101

Paper ID: 16042

Time Allowed: 02 Hours **Max. Marks: 60**

NOTE:

1) Each question is of 10 marks.
2) Attempt any six questions out of nine
3) Any missing data may be assumed appropriately

20-07-21(E)

Q1. a) Convert decimal 27.125 to octal
b) Convert 225.225 to binary, octal and hexadecimal

Q2. Distinguish between a) Combinational and sequential circuit b) Multiplexer and De-multiplexer

Q3. Define De-Morgan theorem. Prove that if A + B= A+ C and AB=AC', then B=C

Q4. Convert SR flip flop into JK flip flop. Show all the tables involved.

Q5. What is a multiplexer tree? Why is it needed? Draw the block diagram of a 32:1 multiplexer tree and explain how input is directed to the output in this system.

Q6. Design a 3 bit synchronous Up/Down Counter.

Q7. Why we need A/D techniques? A 4 bit D/A converter have an output range of '0 to 1.5V. Define its resolution.

Q8. Design a full adder circuit. Distinguish between level triggering and edge triggering.

Q9. What is the reasoning for modelling in VHDL? Write a program in VHDL to show the working of AND gate.

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P.T.O.

EVENING

10 MAR 2021

Please check that this question paper contains 9 questions and 2 printed pages within first ten minutes.

[Total No. of Questions: 09] [Total No. of Pages: ..2....]

Uni. Roll No. .....

Program: B.Tech. (Batch 2018 onward)
Semester: 3
Name of Subject: Digital Circuits and Logic Design
Subject Code: ESIT-101
Paper ID: 16042

Time Allowed: 03 Hours **Max. Marks: 60**

NOTE:

1) Parts A and B are compulsory
2) Part-C has Two Questions Q8 and Q9. Both are compulsory, but with internal choice
3) Any missing data may be assumed appropriately

Part – A **[Marks: 02 each]**

Q1.

a) What is De-Morgan's Theorem? (LOTS)

b) What is decoder? Compare decoder and demultiplexer with suitable block diagram. (LOTS)

c) Explain the term resolution and accuracy of A/D convertors. (LOTS)

d) What is the difference between a latch and a flip flop. (LOTS)

e) Perform Subtraction using 2's Complement: $(101001)_2 - (001100)_2$ (HOTS)

f) Add the following decimal numbers using BCD Addition and verify your result: 599 and 984 (HOTS)

Part – B **[Marks: 04 each]**

Q2. Minimize the following expressions using Boolean algebra: (LOTS)

1) A'.B.C+ A.B'.C + A.B.C' + ABC

2) (ABC)' (A + C) (A + C')

Q3. Implement full adder using two half adders and one OR gate. (LOTS)

Q4. What is Race around condition? How it can be avoided? Also discuss the working of Master Slave J-K Flip Flop. (LOTS)

Q5. Explain the working of 3-bit shift register. (HOTS)

Q6. Design 4-to-16 decoder with 2-to-4 decoder. (HOTS)

P.T.O.

Q7. Draw the circuit of BCD adder and explain it. (HOTS)

Part – C **[Marks: 12 each]**

Q8. Simplify the minterm expression for F : F(P,Q,R,S) = ∑ (0,2,5,7,8,10,13,15) using K-Map. The minterms 2, 7, 8 and 13 are 'do not care' terms. (LOTS)

OR

What are universal gates and why they are called so? Impement AND, OR, NOT and XOR gates using NAND gates. (LOTS)

Q9. Design a combinational circuit to implement a 4-bit Binary to Gray code convertor. (HOTS)

OR

Differentiate between synchronous and asynchronous counters. Design 3-bit synchronous up counter using T flip flops. (HOTS)

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Please check that this question paper contains ___09__ questions and _2_____ printed pages within first ten

[Total No. of Questions: 09]
Uni. Roll No. 2203844

[Total No. of Pages: ...02...]

Program: B.Tech. (Batch 2018 onward)
Semester: 3rd
Name of Subject: Digital Circuits and Logic Design
Subject Code: ESIT-101
Paper ID: 16042

Time Allowed: 03 Hours **Max. Marks: 60**

NOTE:

1) Parts A and B are compulsory
2) Part-C has Two Questions Q8 and Q9. Both are compulsory, but with internal choice
3) Any missing data may be assumed appropriately

Part – A **[Marks: 02 each]**

Q1.

a. Convert the binary number 11010101 into its corresponding hexadecimal form.
b. State De- Morgan's Theorem.
c. What are the various uses of VHDL?
d. How multiplexer different from decoder?
e. Differentiate Moore and Mealy circuits.
f. Define race condition in JK flip flop

Part – B **[Marks: 04 each]**

Q2. Define 2's complement. Subtract $(1010)_2$ from $(1000)_2$ using 2's complement method.
Q3. Write a note on RTL logic family.
Q4. Illustrate the working of Master Slave J-K flip flop.
Q5. Explain the full adder circuit using logic diagram and Truth Table.
Q6. Describe the working of Johnson Ring Counter.
Q7. Illustrate the operation of basic flip-flop using NOR gates.

P.T.O.

Part – C

[Marks: 12 each]

Q8. Write short note on following:

a) Successive approximation A to D conversion technique (6 marks)

b) Ripple Carry Adder (6 marks)

OR

Explain different logic gates families in digital circuits. Write a short note on Universal Gate.

Q9. Design 2-bit Synchronous Up counter using JK flip flop.

OR

Minimise the following function in SOP minimal form using K-Maps:
F (A, B, C, D) = m (1, 2, 6, 7, 8, 13, 14, 15) + d (0, 3, 5, 12)

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Please check that this question paper contains 09 questions and 01 printed pages within first ten minutes.

[Total No. of Questions: 09] [Total No. of Pages: 01]

Uni. Roll No. …….

Program: B.Tech. (IT)
Semester: 3rd
Name of Subject: Digital Circuits and Logic Design
Subject Code: ESIT-101
Paper ID: 16042

Time Allowed: 02 Hours **Max. Marks: 60**

NOTE:

1) Each question is of 10 marks.
2) Attempt any six questions out of nine
3) Any missing data may be assumed appropriately

20-07-21(E)

Q1. a) Convert decimal 27.125 to octal
b) Convert 225.225 to binary, octal and hexadecimal

Q2. Distinguish between **a)** Combinational and sequential circuit **b)** Multiplexer and De-multiplexer

Q3. Define De-Morgan theorem. Prove that if A + B= A+ C and AB=AC , then B=C

Q4. Convert SR flip flop into JK flip flop. Show all the tables involved.

Q5. What is a multiplexer tree? Why is it needed? Draw the block diagram of a 32:1 multiplexer tree and explain how input is directed to the output in this system.

Q6. Design a 3 bit synchronous Up/Down Counter.

Q7. Why we need A/D techniques? A 4 bit D/A converter have an output range of '0 to 1.5V. Define its resolution.

Q8. Design a full adder circuit. Distinguish between level triggering and edge triggering.

Q9. What is the reasoning for modelling in VHDL? Write a program in VHDL to show the working of AND gate.

****

P.T.O.

EVENING

10 MAR 2021

Please check that this question paper contains 9 questions and 2 printed pages within first ten minutes.

[Total No. of Questions: 09] [Total No. of Pages: ..2....]

Uni. Roll No. .....

Program: B.Tech. (Batch 2018 onward)
Semester: 3
Name of Subject: Digital Circuits and Logic Design
Subject Code: ESIT-101
Paper ID: 16042

Time Allowed: 03 Hours **Max. Marks: 60**

NOTE:

1) Parts A and B are compulsory
2) Part-C has Two Questions Q8 and Q9. Both are compulsory, but with internal choice
3) Any missing data may be assumed appropriately

Part – A **[Marks: 02 each]**

Q1.

a) What is De-Morgan's Theorem? (LOTS)

b) What is decoder? Compare decoder and demultiplexer with suitable block diagram. (LOTS)

c) Explain the term resolution and accuracy of A/D convertors. (LOTS)

d) What is the difference between a latch and a flip flop. (LOTS)

e) Perform Subtraction using 2's Complement: $(101001)_2 - (001100)_2$ (HOTS)

f) Add the following decimal numbers using BCD Addition and verify your result: 599 and 984 (HOTS)

Part – B **[Marks: 04 each]**

Q2. Minimize the following expressions using Boolean algebra: (LOTS)

1) A'.B.C+ A.B'.C + A.B.C' + ABC

2) (ABC)' (A + C) (A + C')

Q3. Implement full adder using two half adders and one OR gate. (LOTS)

Q4. What is Race around condition? How it can be avoided? Also discuss the working of Master Slave J-K Flip Flop. (LOTS)

Q5. Explain the working of 3-bit shift register. (HOTS)

Q6. Design 4-to-16 decoder with 2-to-4 decoder. (HOTS)

P.T.O.

Q7. Draw the circuit of BCD adder and explain it. (HOTS)

Part – C **[Marks: 12 each]**

Q8. Simplify the minterm expression for F : F(P,Q,R,S) = $\sum$ (0,2,5,7,8,10,13,15) using K-Map. The minterms 2, 7, 8 and 13 are 'do not care' terms. (LOTS)

OR

What are universal gates and why they are called so? Impement AND, OR, NOT and XOR gates using NAND gates. (LOTS)

Q9. Design a combinational circuit to implement a 4-bit Binary to Gray code convertor. (HOTS)

OR

Differentiate between synchronous and asynchronous counters. Design 3-bit synchronous up counter using T flip flops. (HOTS)

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Please check that this question paper contains 9 questions and 2 printed pages within first ten minutes.

[Total No. of Questions: 09]
Uni. Roll No. .....

[Total No. of Pages: 2...]

Program: B.Tech. (Batch 2018 onward)
Semester:.....3rd.....
Name of Subject: Digital Circuits and Logic Design
Subject Code: ...ESIT-101.....
Paper ID: ...16042....
Scientific calculator is Allowed

MORNING
09 MAY 2023

Time Allowed: 03 Hours **Max. Marks: 60**

NOTE:

1) Parts A and B are compulsory
2) Part-C has Two Questions Q8 and Q9. Both are compulsory, but with internal choice
3) Any missing data may be assumed appropriately

Part – A

[Marks: 02 each]

Q1.

Q1. a) What are ASCII codes.

b) What is the difference between Multiplexer and Demultiplexer.

c) Differentiate between Flip flop and Register.

d) Give the use of VHDL.

e) State and prove De Morgan's theorem.

f) Why NAND and NOR are called universal gates?

Part – B

[Marks: 04 each]

Q2) Why Gray codes are used in K-Maps. Explain in detail

Q3) Convert the following:

a) $(331)_8 = (\ )_{16} = (\ )_{10}$

b) $(11001010)_2 = (\ )_{\text{Gray code}}$

c) $(111)_2 = (\ )_{\text{BCD}}$

d) $(1101)_2 + (1110)_2 = (\ )_8$

P.T.O.

Q4) Simplify following expressions using Boolean algebra

a) F(P,Q,R)=P'Q+QR'+QR+PQ'R'

b) F(X,Y,Z)= X'Y'Z'+X'YZ'+X'YZ+XYZ'

MORNING

09 MAY 2023

Q5) What is SOP and POS in digital circuits? Explain in detail.

Q6) Using Universal gates, create following gates

a) XOR b) AND

Q7) Design 2 bit Encoder and Decoder circuit

Part – C **[Marks: 12 each]**

Q8) Design 3 bit Synchronous Up Counter.

OR

Simplify the given K-Map

cd \ ab	00	01	11	10
00	1	X	X	1
01	X			1
11				
10	1			X

Q9) What are various techniques to convert Analog to Digital signals? Explain any one in detail.

OR

Demonstrate the working of Master Slave flip-flop in detail.

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Please check that this question paper contains___9___ questions and __2____ printed pages within first ten

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Uni. Roll No. …….

Program: ……B.Tech……

Semester:.....3.....

Name of Subject: Digital Circuits and Logic Design

Subject Code: …ESIT-101…..

Paper ID: …16042...

Time Allowed: 02 Hours **Max. Marks: 60**

NOTE:

1) Each question is of 10 marks.
2) Attempt any six questions out of nine
3) Any missing data may be assumed appropriately

07-01-2022(M)

1) Simplify following expressions using Boolean algebra
   a) F(P,Q,R)=P'Q+QR'+QR+PQ'R'
   b) F(X,Y,Z)= X'Y'Z'+X'YZ'+X'YZ+XYZ'

2) Design 1 bit full adder using Multiplexer.

3) Provide minimized SOP expression for the following K-Map

1	0	0	1
0	d	0	0
0	0	d	1
1	0	0	1

4) Convert following:

a) $(331)_8 = (\ )_{16} = (\ )_{10}$

b) $(11001010)_2 = (\ )_{\text{Gray code}}$

c) $(111)_2 = (\ )_{\text{BCD}}$

d) $(1101)_2 + (1110)_2 = (\ )_8$

5) Design 3 bit Synchronous Down Counter.

6) Simplify K-Map

cd \ ab	00	01	11	10
00	**1**	**X**	**X**	**1**
01	**X**			**1**
11				
10	**1**			**X**

7) What are various techniques to convert Analog to Digital signals? Explain any one in detail.

8) Prove the following using Boolean algebra:

a) PQ + P'R + QR = PQ + P'R

b) XY+ X'Z = (X+Z) (X'+ Y)

9) a) Explain working of Even parity generator with circuit diagram.

b) Why gray codes are used in K-Maps. Explain in detail.

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MORNING

27 DEC 2022

Program: B.Tech. (Batch 2018 onward)

Semester: 3rd

Name of Subject: Digital Circuits and Logic Design

Subject Code: ESIT-101

Paper ID: 16042

Time Allowed: 03 Hours **Max. Marks: 60**

NOTE:

1) Parts A and B are compulsory
2) Part-C has Two Questions Q8 and Q9. Both are compulsory, but with internal choice
3) Any missing data may be assumed appropriately

Part – A **[Marks: 02 each]**

Q1.

a) Define 1's complement and 2's complement.

b) What are the various uses of VHDL?

c) Illustrate the advantages of Ring Counter.

d) Write a short note on SOP and POS.

e) Convert $(10101)_2$ to decimal.

f) Compare encoder and decoder.

Part – B **[Marks: 04 each]**

Q2. State and prove De-Morgan's Theorem.

Q3. What are universal gates? Realize the following gates using universal gates:

a. AND b. EX-NOR

Q4. Illustrate the working of Master Slave J-K flip flop.

Q5. Reduce the following Boolean expression: x'y'z +yz+ xz.

Q6. What is full subtractor? Draw a full subtractor circuit.

Q7. Explain the working of Gray code. Write its importance and its uses.

Part – C **[Marks: 12 each]**

Q8. Write short note on following:

a. RTL logic family **(6 marks)**

b. R-2R Ladder **(6 marks)**

OR

Design an 8 ×1 multiplexer using 4×1 and 2×1 multiplexer.

Q9. Design 2-bit Synchronous Up counter using JK flip flop.

OR

Minimize the following Boolean function-

$$F(A, B, C, D) = \Sigma m(1, 3, 4, 6, 8, 9, 11, 13, 15) + \Sigma d(0, 2, 14)$$

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